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IBM 9020D and 9020E System Principles of Operation

This manual is a comprehensive presentation of the characteristics, functions, and features of the IBM 9020 D/E System.

The manual defines 9020 D/E System operating principles, computing and Input/Output Control elements, instructions, System control and monitoring facilities, branching, status switching, interruption system, and input/output operations.

Descriptions of specific input/output devices used within the 9020 D/E System appear in separate publications.

For additional information concerning units attached to the 9020D or 9020E, reference should be made to specific interface control documents.

APPENDIX G. SYSTEM/360 MODE OF OPERATION

SUBSYSTEM DEFINITION

One simplex subsystem whose operation is compatible with IBM System/360 architecture (as defined in IBM System/360 Principles of Operation, Form A22-6821), may be configured from any IBM 9020D or 9020E System. Such a subsystem contains:

... One IBM 7201-02 Computing Element (CE)

... One IBM 7231-02 Input/Output Control Element (IOCE-1)

... One or more IBM 7251-09 Storage Element (SE)

The subsystem may include the following peripheral elements, assigned to IOCE-1 through an IBM 7265-02 System Console (SC) on a 9020D System or IBM 7265-03 Configuration Console (CC) on a 9020E System:

... IBM 2821-1 Control Unit

... IBM 2540 Card Read/Punch

... IBM 1403-2 Printer

... IBM 1052 System Console Printer Keyboard

A subsystem may also include IBM 2803-01 Tape Control Units and the available IBM 2401-2/3 Magnetic Tape Units, and up to three IBM 2314 Storage Control Units and the available IBM 2312 or 2318 Disk Storage Units.

MODE SWITCHING

Any CE in state One or Zero may be switched from "9020-mode" operation to "360-mode" by pressing a back-lighted mode change switch provided on its control panel (Chapter 11). A CE in "360-mode" is returned to "9020-mode" by pressing the mode change switch, by a power-on reset, by receipt of an external start signal from another CE, or by placing it in state Two or Three.

PROGRAMMING NOTE

A CE in "360-mode" is returned to "9020-mode" whenever it is placed in either state Two or Three. This occurs when it is configured to state Two or Three by another CE executing SET CONFIGURATION (section 8.4.5.4), or when recalled to state Three by a CE-ELC (section 9.5.3.2). Similarly, system IPL and system PSW restart force a CE into state Three and thus always take it out of "360-mode".

INSTRUCTION REPERTOIRE

The following operation codes are not assigned for execution in "360-mode". When any of these instructions are encountered an operation code exception is recognized, and a program interruption is taken. The operation is suppressed.

Operation Code	Name	Mnemonic	Section
01	SET CONFIGURATION	SCON	8.4.5.4
02	CONVERT and SORT SYMBOLS	CSS	8.6.1.2
03	CONVERT WEATHER LINES	CVWL	8.6.1.3
0B	DELAY	DLY	8.4.5.1
0C	LOAD IDENTITY	LI	8.4.5.2
0D	SET ADDRESS TRANSLATOR	SATR	8.4.5.7
0E	INSERT ADDRESS TRANSLATOR	IATR	8.4.5.8
0F	REPACK SYMBOLS	RPSB	8.6.1.4
52	LOAD CHAIN	LC	8.6.1.1
9A	START I/O PROCESSOR	SIOP	8.4.5.10
9B	SET PCI	SPCI	10.2.7.5
A0	STORE PS BASE ADDRESS	SPSB	8.4.5.5
A1	LOAD PS BASE ADDRESS	LPSB	8.4.5.3
D8	MOVE WORD	MVW	8.4.5.9

DIRECT-ADDRESS RELOCATION

When a CE is placed in "360-mode" the "logical" preferential-storage base address register (PSBAR) is reset to all zeros. The value in "physical" PSBAR is determined by the identifier appearing in position 1 of the address translator (ATR). Since LOAD PREFERENTIAL-STORAGE BASE ADDRESS cannot be executed, "logical" PSBAR will remain reset unless modified by a subsystem IPL, or subsystem PSW restart.

PSBAR "stepping" and the issuing of a logout-stop signal to a storage element is inhibited in "360-mode" by forcing on the inhibit logout-stop (ILOS) condition in both the CE and IOCE-1.

PREFERENTIAL-STORAGE AREA ASSIGNMENT

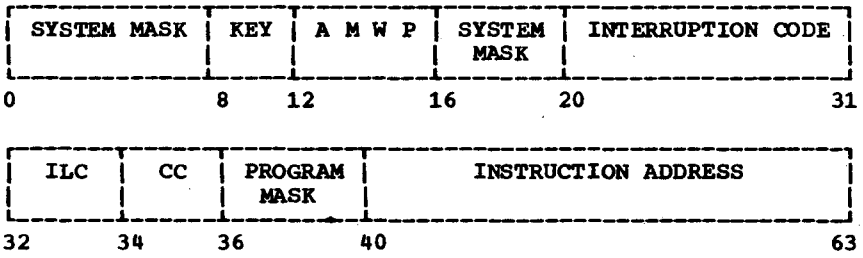
The preferential storage area assignment for both "9020-mode" and "360-mode" is shown in Section 9.1.2 and Table 12-II. The 9020 System is compatible with System/360 in the use of the first 32 words (bytes 000-127 inclusive) of the preferential-storage area. The diagnostic area extends from byte location 128 through byte location 511 in both modes of operation.

PROGRAM STATUS WORD

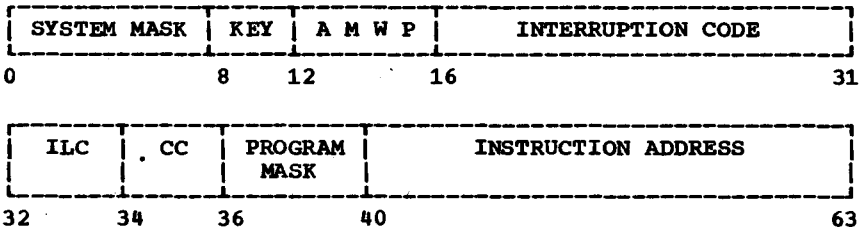
In "9020-mode" operation bits 0-7 and 16-19 of the PSW are interpreted as a 12-bit system mask. In "360-mode" operation the IBM System/360 PSW format applies. Bits 0-7 become the system mask and bits 16-19 are interpreted as the high-order positions of a 16-bit interrup-

tion code field.

IBM 9020 System PSW Format



IBM System/360 PSW Format



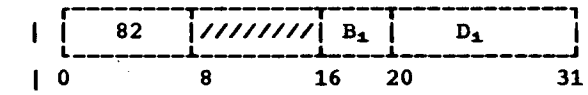
"9020-mode"		"360-mode"
0 - 7	System Mask	
0	Multiplexor Channel A mask	Multiplexor channel mask
1	Selector channel 1A mask	Selector channel 1 mask
2	Selector channel 2A mask	Selector channel 2 mask
3	Selector channel 3A mask	Selector channel 3 mask
4	Multiplexor channel B mask	
5	Selector channel 1B mask	Ignored
6	Selector channel 2B mask	
7	External mask	External mask
8-11	Protection key	
12	USASCII-8 Mode (A)	
13	Machine Check mask (M)	
14	Wait State (W)	
15	Problem State (P)	
16-19	System Mask	16-19 Interruption Code
16	Selector Channel 3B mask	
17	Multiplexor channel C	
18	Selector channel 1C mask	
19	Selector channel 2C mask	
20-31	Interruption Code	
32-33	Instruction length code (ILC)	
34-35	Condition code (CC)	
36-39	Program mask	
36	Fixed-point overflow mask	
37	Decimal overflow mask	
38	Exponent underflow mask	
39	Significance mask	
40-63	Instruction address	

STATUS-SWITCHING INSTRUCTIONS

The instructions LOAD PSW (Section 8.5.1.1), SET SYSTEM MASK (Section 8.5.1.3), and SUPERVISOR CALL (Section 8.5.1.4) are executed as defined for IBM System/360 by a CE operating in "360-mode".

LOAD PSW

| LPSW $D_1(B_1)$ [SI]



The double word at the location designated by the operand address replaces the PSW.

The operand address must have its three low-order bits zero to designate a double word; otherwise a specification exception results in a program interruption.

The double word which is loaded becomes the PSW for the next sequence of instructions. Bits 40-63 of the double word become the new instruction address. The new instruction address is not checked for available storage or for an even byte address during a load PSW operation. These checks occur as part of the execution of the next instruction.

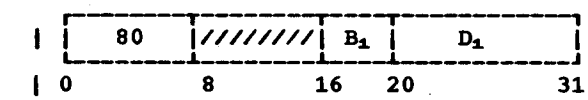
Bits 8-11 of the double word become the new protection key. The interruption code in bit positions 16-31 of the new PSW is not retained as the PSW is loaded. When the PSW is subsequently stored because of an interruption, these bit positions contain a new code. Similarly bits 32 and 33 of the PSW are not retained upon loading. They will contain the instruction-length code for the last-interpreted instruction when the PSW is stored during a branch-and-link operation, or during a program or supervisor-call interruption.

Condition Code: The code is set according to bits 34 and 35 of the new PSW loaded.

Program Interruptions:
Privileged operation
Addressing
Specification
Protection

SET SYSTEM MASK

| SSM $D_1(B_1)$ [SI]



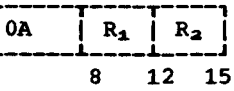
The byte at the location designated by the operand address replaces the system mask, bits 0-7, of the current PSW.

Condition Code: The code remains unchanged.

Program Interruptions:
Privileged operation
Addressing
Protection

SUPERVISOR CALL

| SVC R_1,R_2 [RR]



The instruction causes a supervisor-call interruption, with the R1 and R2 field of the instruction providing the interruption code.

The contents of bit positions 8-15 of the instruction are placed in bit positions 24-31 of the old PSW which is stored in the course of the interruption. Bit positions 16-23 of the old PSW are made zero. The old PSW is stored at location 32 of the preferential-storage area, and a new PSW is obtained from location 96. The instruction is valid in both problem and supervisor state.

Condition Code: The code remains unchanged in the old PSW.

Program Interruptions: None.

INTERRUPTION HANDLING

An interruption consists of storing the current PSW as an "old PSW" and fetching a "new" PSW. Processing resumes in the state indicated by the "new" PSW. To permit proper programming action following an interruption, the cause of the interruption is identified by the interruption code stored in the "old" PSW. In "360-mode" bits 16-31 of the PSW are stored as the interruption code. In "9020-mode" bits 20-31 are stored (Chapter 9). Both interruption codes are shown in the following tabulations.

PROGRAM INTERRUPTIONS

"9020-mode" Interruption Source Identification	Interruption Code PSW Bits		"360-mode" Interruption Source Identification
	<----"360-mode"----->		
		<-"9020-mode"->	
Operation	0000	0000 00000001	Operation
Privileged operation	0000	0000 00000010	Privileged operation
Execute	0000	0000 00000011	Execute
Protection	0000	0000 00000100	Protection
Addressing	0000	0000 00000101	Addressing
Specification	0000	0000 00000110	Specification
Data	0000	0000 00000111	Data
Fixed-point overflow	0000	0000 00001000	Fixed-point overflow
Fixed-point divide	0000	0000 00001001	Fixed-point divide
Decimal overflow	0000	0000 00001010	Decimal overflow
Decimal divide	0000	0000 00001011	Decimal divide
Exponent overflow	0000	0000 00001100	Exponent overflow
Exponent underflow	0000	0000 00001101	Exponent underflow
Significance	0000	0000 00001110	Significance
Floating-point divide	0000	0000 00001111	Floating-point divide
IOCE-3 PSA lockout		0000 00010000	
IOCE-2 PSA lockout		0000 00100000	
IOCE-1 PSA lockout		0000 01000000	
SE stopped		0000 10000000	

Legend

PSA -- Preferential-storage area

PROGRAMMING NOTE

IOCE PSA lockout and SE stopped interruption requests are ignored by a CE in "360-mode". The detection of either condition causes the CE to check stop.

SUPERVISOR CALL INTERRUPTION

"9020-mode Interruption Source Identification	Interruption Code PSW Bits		"360-mode" Interruption Source Identification
	<----"360-mode"----->		
		<-"9020-mode"->	
Instruction bits	0000	0000 rrrrrrrr	Instruction bits

Legend

r -- Bits of R_1 and R_2 field of SUPERVISOR CALL

EXTERNAL INTERRUPTIONS

"9020-mode" Interruption Source Identification	Interruption Code PSW Bits		"360-mode" Interruption Source Identification
	<----"360-mode"----->		
		<-"9020-mode"->	
DAR	0000	xxxx xxxxxxx1	DAR
PIR	0000	xxxx xxxxxx1x	PIR
CE4 Write Direct	0000	xxxx xxxxx1xx	CE4 Write Direct
CE4 Read Direct	0000	xxxx xxxx1xxx	CE4 Read Direct
CE3 Write Direct	0000	xxxx xxx1xxxx	CE3 Write Direct
CE3 Read Direct	0000	xxxx xx1xxxxx	CE3 Read Direct
Interrupt Switch	0000	xxxx x1xxxxxx	Interrupt Switch
Timer	0000	xxxx 1xxxxxxx	Timer
CE2 Write Direct	0000	xxx1 xxxxxxxx	CE2 Write Direct
CE2 Read Direct	0000	xx1x xxxxxxxx	CE2 Read Direct
CE1 Write Direct	0000	x1xx xxxxxxxx	CE1 Write Direct
CE1 Read Direct	0000	1xxx xxxxxxxx	CE1 Read Direct

Legend

x -- Unpredictable

DAR -- Diagnose accessible register
PIR -- Processor interrupt register

PROGRAMMING NOTE

The direct control instructions READ DIRECT and WRITE DIRECT are defined for 9020 System operation (Chapter 8). They are executed in "360-mode" subject to all the conditions placed on them in "9020-mode". In particular, specification exceptions and condition code settings can occur which are not part of System/360 architecture.

INPUT/OUTPUT INTERRUPTIONS

"9020-mode" Interruption Source Identification	Interruption Code PSW Bits		"360-mode" Interruption Source Identification
	<----"360-mode"----->		
		<-"9020-mode"->	
Multiplexor Channel A	0000	0000 aaaaaaaa	Multiplexor Channel
Selector Channel 1A	0000	0001 aaaaaaaa	Selector Channel 1
Selector Channel 2A	0000	0010 aaaaaaaa	Selector Channel 2
Selector Channel 3A	0000	0011 aaaaaaaa	* Selector Channel 3
Multiplexor Channel B		0100 aaaaaaaa	
Selector Channel 1B		0101 aaaaaaaa	
Selector Channel 2B		0110 aaaaaaaa	
Selector Channel 3B		0111 aaaaaaaa	
Multiplexor Channel C		1000 aaaaaaaa	
Selector Channel 1C		1001 aaaaaaaa	
Selector Channel 2C		1010 aaaaaaaa	

Legend

a -- Device Address Bit

* -- Optional Channel in IOCE-1

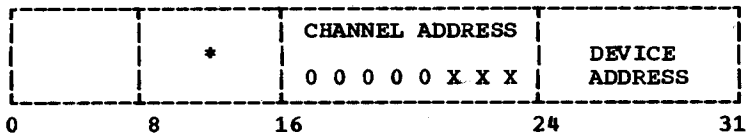
MACHINE-CHECK INTERRUPTIONS			
"9020-mode Interruption Source Identification	Interruption Code PSW Bits		"360-mode" Interruption Source Identification
	<----"360-mode"----->		
		<-"9020-mode"->	
CE Malfunction	0000	0000 00000000	CE Malfunction
IOCE-1 Malfunction	0000	0000 00000001	IOCE-1 Malfunction
IOCE-2 Malfunction		0000 00000010	
IOCE-3 Malfunction		0000 00000011	
Read Direct Timeout	0000	0000 00000100	Read Direct Timeout

INPUT/OUTPUT

Input/Output Addressing

Channel and device addresses are developed as the sum obtained by the addition of the content of register B_1 and the content of the D_1 field of the I/O instruction being executed.

This sum has the format:



Bit positions 0-7 are not part of the address. Bit positions 8-15, which constitute the high-order portion of the address are ignored. Bit positions 16-23 of the sum contain the channel address, while bit positions 24-31 identify the device on the channel.

Bit positions 16-20 of the sum must contain zeros. A condition code 3 is set for an I/O instruction that does not contain the proper number of zeros. Instruction execution is terminated.

Channel Addressing

Channel Address	"9020-mode" Interpretation	"360-mode" Interpretation
0000 0000	Multiplexor Channel A	Multiplexor Channel
0000 0001	Selector Channel 1A	Selector Channel 1
0000 0010	Selector Channel 2A	Selector Channel 2
0000 0011	Selector Channel 3A	Selector Channel 3
0000 0100	Multiplexor Channel B	Not operational
0000 0101	Selector Channel 1B	Not operational
0000 0110	Selector Channel 2B	Not operational
0000 0111	Selector Channel 3B	Invalid
0000 1000	Multiplexor Channel C	Invalid
0000 1001	Selector Channel 1C	Invalid
0000 1010	Selector Channel 2C	Invalid
0000 1011 thru 1111 1111	Invalid	Invalid

PROGRAMMING NOTE

A subsystem configured for "360-mode" operation uses IOCE-1. Consequently, I/O instructions which specify other channels are terminated with condition code 3 stored to indicate that the addressed channel is not operational, or that the channel address is invalid.

INITIAL PROGRAM LOADING

System IPL cannot be carried out in "360-mode" as the CE is forced into state Three which causes it to return to "9020-mode". A 9020

system IPL takes place (Chapter 11). Similar action occurs when a system PSW restart is attempted in "360-mode".

A subsystem IPL, or subsystem PSW restart may be carried out in "360-mode". Both "logical" and "physical" PSBARS are set to reference the SE designated in the main storage select switch. The first PSW is fetched from location 0 in this SE.

STORAGE PROTECTION

For protection purposes main storage is divided into blocks of 2048 bytes, each block having an address which is a multiple of 2048. A five-bit storage key is associated with each block. When data are stored in a storage block, the four high-order bits of the storage key are compared with the protection key. When data are fetched the fetch-protection bit (fifth, i.e., low-order bit) is inspected. When the fetch-protection bit is one the four high-order bits of the storage key are compared with the protection key. The protection key of the current PSW is used as the comparand when a storage access is specified by an instruction. When a storage access is specified by a channel operation, the protection key supplied to the channel by the CAW is used as the comparand.

The keys are said to match in either "9020-mode" or "360-mode" when they are equal or when either one is zero. This operation is not compatible with IBM System/360 architecture, as the keys are said to match in System/360 when they are equal or when the protection key is zero.

Protection Key	Storage Key	9020 System Interpretation	System/360 Interpretation
X	X	Match	Match
X	Y	Mismatch	Mismatch
X	Zero	Match	Mismatch
Zero	X	Match	Match
Zero	Zero	Match	Match

Where X ≠ zero, Y ≠ zero.

IOCE-PROCESSOR OPERATION

The IOCE-processor capability is disabled when an IOCE (applicable to IOCE-1 only) is placed in "360-Mode". The IOCE-processor is forced into the stopped state by hardware. "360-Mode" operation is unchanged.